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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,226	06/26/2003	Hideaki Watanabe	024016-00063	3751

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EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,226	WATANABE, HIDEAKI	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 14-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14 and 17-21* is/are rejected.

7)☒ Claim(s) *15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 3 and 20 are objected to because of the following informalities: the recitation "wherein the counter is **counter** for obtaining..." is not clear. It should be "wherein the counter is a counter for obtaining..."; the recitation "a DA converter for converts the difference..." in claim 20 should be "a DA converter for converting the difference...".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 20 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 20, the recitation "an analog integration circuit for integrating the analog difference voltage to thereby obtain the analog control voltage " is indefinite because it is misdescriptive. The drawings of the present application show that the output of the DAC is the analog control voltage that is applied **directly** to the VCO. There is no "an analog integration circuit" and "analog difference voltage" seen. The Applicant is requested to point out in the drawing the circuit of claim 20 and the "an analog integration circuit" and to show how the "analog difference voltage" is generated.

Regarding claim 21, the recitation "integration means for integrating the count value **either** digitally or analogically" is indefinite because it is misdescriptive. The drawings of the present application shows that the "integration means" comprises digital components (subtracter, adder) and a "DAC" that converts a digital input to an analog output. There is no circuit (means) that functions as a digital circuit or an analog circuit that integrates the signal seen. The Applicant is requested to point out in the drawing the "integration means".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-12, 14, and 17-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Kokubo et al. (US Pat. 5,928,208).

Regarding claim 1, figure 11 of Kokubo shows a clock multiplication circuit for delivering an output clock signal at a frequency that is a multiple of the frequency of a reference clock signal as inputted, the clock multiplication circuit comprising:

a counter (5) for delivering a count value by counting the number of effective transition edges of the output clock signal, existing during a predetermined counting period given on the basis of the reference clock signal (fref);

a subtracter (17, 6) for delivering a difference value obtained by subtracting either the count value or a reference value from the other;

a control voltage generation circuit (18, 9, 4) for delivering an analog control voltage (Va) corresponding to an integrated value of the difference value comprising an adder (18) for obtaining a new integrated value by adding the difference value to an integrated value obtaining in a preceding counting period and a DA converter (9) circuit for converting the new integrated value into the analog control voltage (col.7, lines 4-11); and

a voltage control oscillator circuit (1) for delivering the output clock signal at a frequency corresponding to the analog control voltage (Va). Note that the bits of the difference value (Nv) is added to existing contents of the accumulator 8 (an integrated value obtaining in a preceding counting period) to obtain a new integrated value (resulting sum). DAC (9) converts the new integrated value into the analog voltage (Va) col. 7, lines 4-11).

Regarding claims 2 and 3, figure 4 lines (E1) and (E2) shows that when the count value (Nv) is greater or smaller that a predetermined value (N), the output of the accumulator register (18) changes values (from 1000 to 0100 and from 1000 to 1100) at the end of the counting period and before the start of a succeeding counting period (the period of the

reference input clock (fref) (see col. 4, lines 1-38). Line (C) of figure 4 shows that the counter counts during the high/low level period.

Regarding claim 4, figure 4 shows that when the signal (B) goes high at the end of the high level period, the current count value (Nv) changes and the digital value in the accumulator register (18) changes thus, the analog control voltage (Va) changes as a result, the frequency of the output clock signal changes before the start of the succeeding low level period (col. 7, lines 10-11).

Regarding claims 5, 6, 7 and 8, figure 11 of Kokubo show that the counter (5) delivers the count value (Nv) after the end of the counting period and in synchronization with the output clock signal, the subtracter (17) delivers the difference value after the end of the counting period and in synchronization with the output clock signal, and the control voltage generation circuit (18, 9, 4) delivers the analog control voltage (Vr) after the end of the counting period and in synchronization with the output clock signal. The clock cycle of signal (fref) including high and low levels controls the functioning of the counter (5). The multiplier (10, 18) comprises a shift register (18).

Regarding claims 9, 10, 11 and 12, controller (10) initializes the multiplier (18) with different digital values (col. 3 lines 60-64). The storage means is element (11).

Regarding claims 14 and 17-19, the initial integrated value acquisition means internal component (18) for acquiring an initial integrated value to be used by the adder (internal to element 18) after the clock multiplication circuit is power on or reset (col. 7, lines 1-11). The memory is element (6).

Regarding claim 20, the control voltage generation circuit comprises a DA converter ((9) that generates the analog control voltage (Va).

Regarding claim 21, figure 2 or 11 of Kokubo shows a clock multiplication circuit for delivering an output clock signal at a frequency that is a multiple of the frequency of a reference clock signal as inputted, the clock multiplication circuit comprising:

a counter (5) for delivering a count value by counting the number of effective transition edges of the output clock signal, existing during a predetermined counting period given on the basis of the reference clock signal (fref);

an oscillation circuit (1) for delivering the output clock signal; and

an oscillation control circuit (6, 7, 8, 9, 4) for controlling the frequency of the output clock signal from the oscillation circuit such that the count value becomes equal to a predetermined reference value. The integration means is a part of the oscillation control circuit.

Allowable Subject Matter

Claims 15 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 15 and 16 are objected to because the prior art of record fails to teach or fairly suggest a clock multiplication circuit comprising a initial integrated value acquisition means as called for in claim 15 and 16.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
11-05-04

TUAN T. LAM
PRIMARY EXAMINER